

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): S.R. Cebenko et al.  
Case: 1-1-3-1-1  
Serial No.: To Be Assigned  
Filing Date: February 14, 2002  
Title: Integrated Circuit Base Transistor Structure  
and Associated Programmable Cell Library  
Group: To Be Assigned  
Examiner: To Be Assigned

Jc971 U.S. PTO  
10/082050  
02/14/02

#4  
6/17/03  
M. Pruden

INFORMATION DISCLOSURE STATEMENT

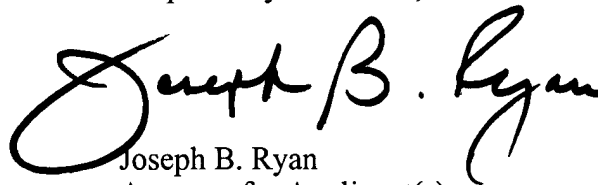
Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants' attorney wishes to bring to the attention of the Patent and Trademark Office the following document listed on the accompanying Form PTO-1449: U.S. Application Serial No. 09/400,029, filed in the name of J.A. Schadt on September 21, 1999 and entitled "Integrated Circuit With Standard Cell Logic and Spare Gates."

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,



Date: February 14, 2002

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Group: TBA

**LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT**

10/082050  
02/14/02

**U.S. PATENT DOCUMENTS**

EXAMINER				FILING DATE
INITIAL	DOCUMENT NO.	DATE	NAME	IF APPROPRIATE
	09/400,029	9/21/99	J.A. Schadt, "Integrated Circuit With Standard Cell Logic and Spare Gates."	

**FOREIGN PATENT DOCUMENTS**

EXAMINER				TRANSLATION	
INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	YES NO

**OTHER DOCUMENTS**

EXAMINER		
INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

Examiner

Date Considered

**Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.